## <u>ABSTRACT</u>

An improved 2-bit boundary scan test circuit capable of applying boundary scan test vectors to the input of the core logic of a circuit, using a multiplexer for selectively coupling the output of a boundary scan register to the input of a boundary scan register or to the input of the core logic, and a selection circuit for controlling the multiplexer to enable the coupling when test vectors are required to be applied to the core.

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